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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,566	06/29/2001	Jun-Cheng Ko	LAM2P258	6944

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EXAMINER	
VINH, LAN	
ART UNIT	**PAPER NUMBER**
1765	7

DATE MAILED: 04/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/895,566	Applicant(s) KO ET AL.	
	Examiner Lan Vinh	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I claims, method claims 1-10, 16-20 in Paper No. 6 is acknowledged. Claims 11-15 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cain (US 5,242,532) in view of Gabriel (US 5,198,072)

Cain discloses a method of plasma endpoint detection etches a designated layer of a specified material on a substrate. This method comprises the steps of:

forming a semiconductor structure 202 having a gate member 210 on/over a surface of the substrate 206 (col 4, lines 14-20, fig. 2A), which reads on forming a gate structure on/over a first surface of the substrate

forming spacers 234 along sidewall of gate structure 210 (col 4, lines 56-57, fig. 2C)

forming source region 246 and drain diffusion region 250 in the surface of the substrate 206 (col 4, lines 65-66, fig. 2C shows that source/drain regions 246 and 250 located/defined outside of the spacer 234

forming a TEOS (tetraethylorthosilicate) layer 402 over the surface of the substrate 206 (col 7, lines 39-40), fig. 5C shows that layer 402 is formed between dielectric layer 410 (BBSG) and the substrate surface and the layer 402 overlies the gate structure 210, the spacers 234 and the surface of the substrate, which reads on forming an interlevel dielectric layer (IDL) directly over the first surface of the substrate without forming a stop layer, such that the IDL layer overlies the gate structure, the spacers and the first surface of the substrate since Cain does not discloses forming a silicon nitride layer (claimed etch stop layer as defined in page 1 of the specification) on the layer 402/dielectric layer

plasma etching through the layer 402/IDL layer, in an plasma chamber, to form an opening 242'/contact hole to the top layer of gate structure 210 and an opening 250' /via hole exposing the source/drain regions (col 7, lines 61-67, col 8, lines 1-2, fig. 5E)

generating an endpoint signal upon completing the etching step (col 8, lines 37-38), which reads on discontinuing the plasma etching process when detecting an endpoint signal.

Unlike the instant claimed inventions as per claims 1 and 6, Cain does not specifically disclose the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

However, Gabriel discloses a method and apparatus for detecting endpoint when etching dielectric layer comprises the step of monitoring DC bias change (voltage rise /step increase) on the cathode 16/substrate (wafer) 42 to terminate the etching of the dielectric layer (col 2, lines 61-62, col 3, lines 67-68, col 4, lines 9-14, fig. 1). Gabriel teaching reads on the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

Since Cain discloses that plasma etcher using endpoint monitoring apparatus sensitive to parameters such as DC bias level may be used to implement the etching process (dielectric etching process) (col 8, lines 56-60), one skilled in the art would have found it obvious to modify Cain method by using the endpoint method as taught per Gabriel since Gabriel states that his invention detects imminent endpoint when plasma etching dielectrics thereby permitting the process to be terminated before the substrate is damaged (col 2, lines 58-60)

Regarding claims 2, 7, Cain discloses that the endpoint signal is generated upon completing etching (col 8, lines 37-40). Fig. 6F shows the etching exposes a portion of the surface of the substrate under the contact hole and a portion of the top layer of the gate structure.

The limitations of claims 3, 4, 5 have been discussed above.

Regarding claim 8, Cain also discloses forming a gate oxide 212 over the surface of the substrate and forming a polysilicon layer 210 over the gate oxide 212 (col 4, lines 16-17, fig. 2A)

Regarding claim 10, Cain discloses forming a spacer layer 234 over the surface of the substrate and the gate structure and plasma etching the spacer layer to form spacer 234 along the sidewall of the gate structure 210 (col 4, lines 14-20, fig. 2C)

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cain (US 5,242,532) in view of Gabriel (US 5,198,072) and further in view of Liaw (US 5,843,815)

Cain as modified by Gabriel has been described above in paragraph 3. Unlike the instant claimed invention as per claim 9, Cain and Gabriel do not disclose depositing an oxide layer over the first surface of the substrate, the gate structure and spacer, depositing a TEOS layer over the oxide and an oxide layer over the TEOS.

However, Liaw discloses a process for forming a MOSFET device/transistor comprises the steps of depositing an oxide layer 10 over the first surface of the substrate, the gate structure and spacer, depositing a TEOS layer 30 over the oxide and an oxide layer 19 over the TEOS (col 4, lines 17-18, col 5, lines 10-24, fig. 7)

Hence, one skilled in the art would have found it obvious to modify Cain and Gabriel by forming an insulating composite structure as per Liaw because according to Liaw a composite interlevel dielectric resulting in a smooth topology (col 5, lines 21-32)

5. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cain (US 5,242,532) in view of Gabriel (US 5,198,072)

Cain discloses a method of plasma endpoint detection etches a designated layer of a specified material on a substrate. This method comprises the steps of:

forming a semiconductor structure 202 having a gate member 210 on/over a surface of the substrate 206 (col 4, lines 14-20, fig. 2A), which reads on providing a substrate having a transistor structure on a surface of the substrate.

forming a TEOS (tetraethylorthosilicate) layer 402 over the surface of the substrate 206 (col 7, lines 39-40), fig. 5C shows that layer 402 is formed between dielectric layer 410 (BPSG) and the substrate surface, which reads on forming a dielectric layer directly over the first surface of the substrate without forming a stop layer since Cain does not discloses forming a silicon nitride layer (claimed etch stop layer as defined in page 1 of the specification) on the layer 402/dielectric layer

plasma etching through the layer 402/dielectric layer, in an plasma chamber, to form an opening 242'/contact hole in the dielectric layer (col 7, lines 61-67, fig. 5E)

introducing reactant/etchant gases into the plasma chamber (col 6, lines 50-60)

activating the power supply to the plasma chamber strikes the plasma and activate the plasma etching process (col 2, lines 11-12)

generating an endpoint signal upon completing the etching step (col 8, lines 37-38), which reads on discontinuing the plasma etching process when detecting an endpoint signal.

Unlike the instant claimed inventions as per claim 16, Cain does not specifically disclose the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

However, Gabriel discloses a method and apparatus for detecting endpoint when etching dielectric layer comprises the step of monitoring DC bias change (voltage rise /step increase) on the cathode 16/substrate (wafer) 42 to terminate the etching of the dielectric layer (col 2, lines 61-62, col 3, lines 67-68, col 4, lines 9-14, fig. 1). Gabriel teaching reads on the step of monitoring a bias compensation voltage (a method used to regulate the voltage present on the wafer as defined in page 14 of the specification) of the plasma processing chamber during the plasma etching and discontinue the plasma etch upon detecting a endpoint signaling change in the bias compensation voltage.

Since Cain discloses that plasma etcher using endpoint monitoring apparatus sensitive to parameters such as DC bias level may be used to implement the etching process (dielectric etching process) (col 8, lines 56-60), one skilled in the art would have found it obvious to modify Cain method by using the endpoint method as taught per Gabriel since Gabriel states that his invention detects imminent endpoint when plasma etching dielectrics thereby permitting the process to be terminated before the substrate is damaged (col 2, lines 58-60).

Regarding claims 17, 20, Cain discloses that the endpoint signal is generated upon completing etching (col 8, lines 37-40). Fig. 5E shows the etching exposes a portion/gate structure 210 under the contact hole 242'

The limitation of claim 18 has been discussed above.

Regarding claim 19, Cain also discloses forming a TEOS (tetraethylorthosilicate) layer 402 over the surface of the substrate 206 (col 7, lines 39-40), fig. 5C shows that layer 402 is formed between dielectric layer 410 (BPSG) and the substrate surface, which reads on forming an interlevel dielectric layer 402.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

LV
March 31, 2003